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Projected Performance of Sub-10 nm GaN-based Double Gate MOSFETs

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ABSTRACT
GaN-based double gate metal-oxide semiconductor field-effect transistors (DG-MOSFETs) in sub-10 nm regime have been designed for the next generation logic applications. To rigorously evaluate the device performance, non-equilibrium Green's function formalism are performed using SILVACO ATLAS. The device is turn on at gate voltage, V_{GS} =1 V while it is going to off at V_{GS} = 0 V. The ON-state and OFF-state drain currents are found as 12 mA/μm and ~10-8 A/μm, respectively at the drain voltage, V_{DS} = 0.75 V. The sub-threshold slope (SS) and drain induced barrier lowering (DIBL) are ~69 mV/decade and ~43 mV/V, which are very compatible with the CMOS technology. To improve the figure of merits of the proposed device, source to gate (S-G) and gate to drain (G-D) distances are varied which is mentioned as underlap. The lengths are maintained equal for both sides of the gate. The SS and DIBL are decreased with increasing the underlap length (L_{UN}). Though the source to drain resistance is increased for enhancing the channel length, the underlap architectures exhibit better performance due to reduced capacitive coupling between the contacts (S-G and G-D) which minimize the short channel effects. Therefore, the proposed GaN-based DG-MOSFETs as one of the excellent promising candidates to substitute currently used MOSFETs for future high speed applications.

Keywords
GaN, DG-MOSFETs, SILVACO, NEGF, drain-induced barrier lowering (DIBL), gate underlap, sub threshold slope (SS).

1. INTRODUCTION
Nano-scaling of metal oxide semiconductor field effect transistors (MOSFETs) has recently been great interest in research activities of CMOS technology to continuously develop the devices more smaller, faster and consume less power for the same level of integration [1-2]. In purpose of increasing ON-state current for better performance the gate length (LG) needs to be shrinked. However, Scaling of MOSFETs to sub-10 nm dimensions it is difficult to maintain the essential device performance due to significantly increased short channel effects (SCEs) [3-5]. The SCEs occur when a fraction of channel escapes gate control due to the influence of junction [6].

Double gate metal oxide semiconductor field effect transistor (DG-MOSFETs) is one of the promising candidate due to its better on-state current and immunity to short channel effects (SCEs) than conventional single gate MOSFETs [7-11]. In sub-10nm regime DG-MOSFETs has good electrostatic gate control over the channel [12]. Though Si based DG-MOSFETs reduces the SCEs [13] have limitations such as low mobility, high gate leakage current, and high delay time [14-16]. In recent, the device drive current increases at lower supply voltage that leads to increase the OFF-state leakage current which causes extraneous standby power dissipation [17]. A new channel material is needed to explore the device structure that would be more energy efficient for high speed switching device. Gallium nitride (GaN) as channel material is an alternative to overcome these limitations because of its low effective mass hence mobility is inversely proportional to carrier effective mass. The GaN material has high thermal stability, high power density and robustness [18]. To overcome the SCEs of GaN-based DG-MOSFETs the underlap length is extended in both source and drain sides that increases the effective channel length, thereby increasing the series resistance in underlap regions. Moreover, using underlap length, in sub-threshold region it reduces gate edge direct tunneling leakage and gate sidewall fringe capacitance due to increasing of effective channel length that ensures better performance. Therefore, it is immense important to design and analysis of logic switching devices. In this work, GaN-based DG-MOSFETs with underlap length have been designed and evaluate their performance for future logic device applications.

2. DEVICE STRUCTURE
The schematic cross-sectional view of simulated GaN-based DG-MOSFETs is shown in Fig. 1. (a) GaN-based DG-MOSFETs without underlap and (b) with underlap length in both gate to source and gate to drain sides. Table I enlists the numerical parameters used for the simulation. We used non-equilibrium Green's function (NEGF) method in the environment of 2D ATLAS TCAD device simulation tool [19]. The device has 10 nm and 9 nm gate length with dielectric hafnium dioxide (HfO_2) having an equivalent oxide thickness (EOT) of 0.59 nm.

Parameter Name	Value
Effective mass of GaN, m*	0.18 m_0
Underlap Length, L_{UN}	0 to 4 nm
Gate length, L_G	10 nm and 9 nm
Gate work function	4.28 eV
N-type Doping Concentration, N_{SD}	1×10^{20} cm^3
P-type Doping Concentration, N_{BODY}	1×10^{15} cm^3

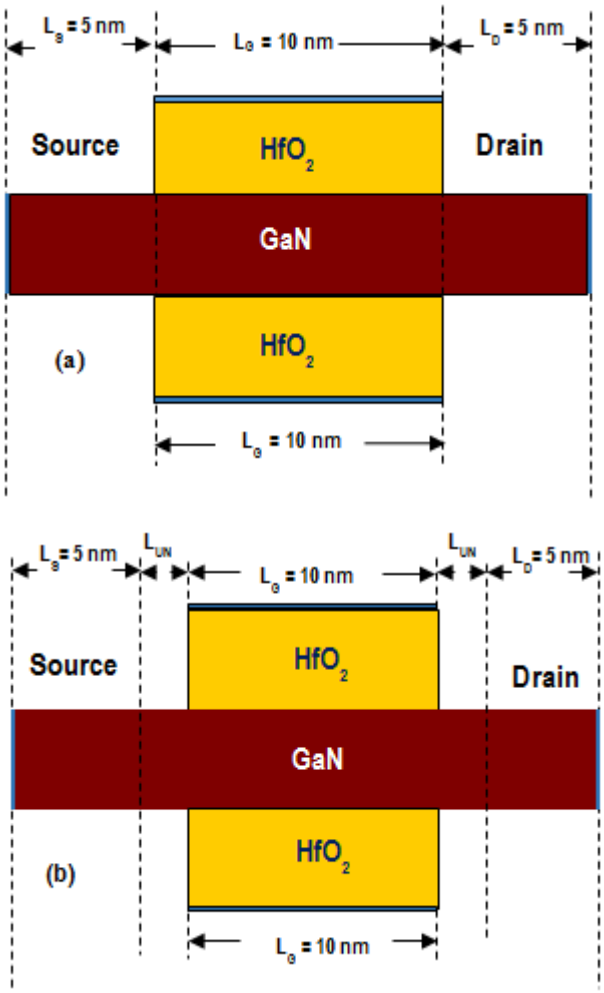

Fig. 1. Schematic of GaN-based DG-MOSFETs (a) without underlap length (b) with underlap length.

3. RESULT ANALYSIS

In this section the simulation results are analyzed. We analyze the performance of GaN-based DG-MOSFETs having gate length of LG = 10 nm and 9 nm, symmetrical underlap lengths varies from LUN = 0 ~ 4 nm on both the gate to source and gate to drain sides. To analyze the device performance the transfer characteristics, ION, IOFF, ION/IOFF ratio, DIBL, sub-threshold slope (SS) are analyzed by varying the underlap length in sub-10 nm regime.

Fig. 2 (a), (b) represents the conduction energy band at OFF-state of 10 nm device ON-state, respectively with different underlap length, 0 ~ 4 nm. Since the device is OFF, the large barrier of p-type channel resists the electrons to flow from source to drain. The barrier is getting increased with increasing the underlap length hence effective channel length increases. Applying gate voltage (1 V) the barrier is reduced hence the electrons flow from source to drain. Since the effective channel length increases with increasing underlap Length, introducing series resistance in the underlap length region that reduces SS for shorter gate length [20]. Thus the short channel effects getting reduced by reducing coupling capacitance.

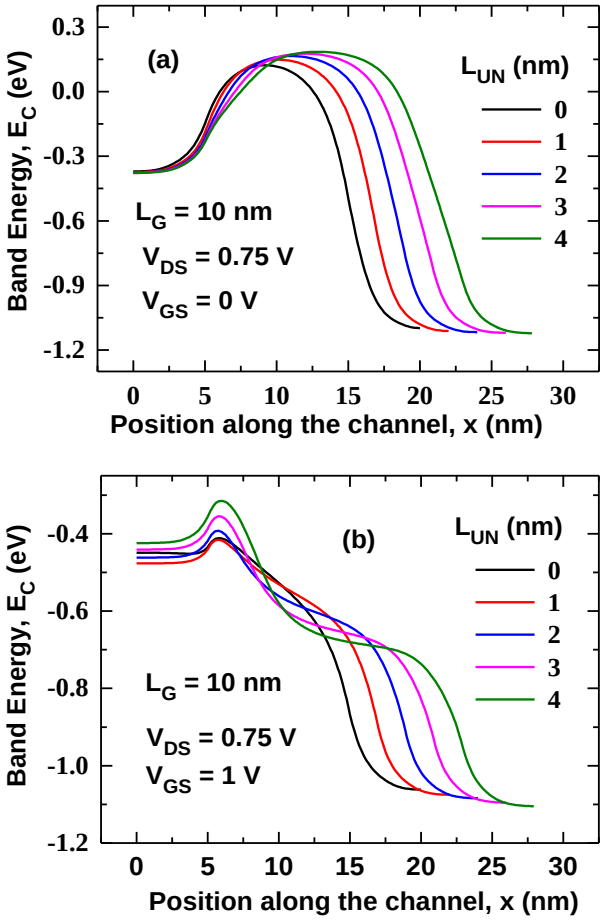

Fig. 2. The conduction band energy while drain voltage 0.75 V of 10 nm gate length device (a) at OFF-state (b) at ON-state.

The transfer characteristics of the GaN-based DG-MOSFETs with different underlap length (LUN = 0 ~ 4 nm) of gate length 10 nm in Fig. 3(a) and of gate length 9 nm in Fig. 3(b). Varying underlap length from 0 nm to 4 nm depicts a very high drain current density (12 mA/μm for LG =10 nm at LUN = 0 nm) arising from the high mobility and velocity of NEGF in the buried channel.

The drain current is decreasing with increasing symmetrical underlap length. Considering lower EOT with double gate MOSFETs, good drain current is observed that provides much better gate control [21]. High electron mobility and conductivity leads to higher drive current at both low drain and high drain bias, which are of great significance for high speed logic applications. The linear drive current (low drain bias) is directly proportional to the conductivity and the saturated drive current (high drain bias) is proportional to the carrier density, as well as the carrier injection velocity. The carrier injection velocity depends on the low field carrier mobility and effective mass m* [22].

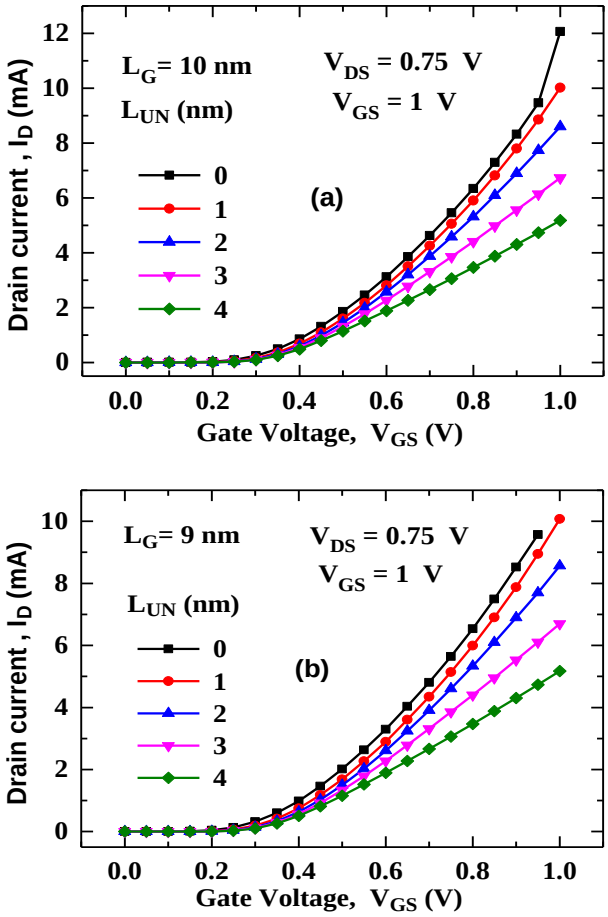

Fig. 3. (a) Transfer characteristics curve for various underlap length (LUN) of 10 nm gate length. (b) of 9 nm gate length. The underlap length (LUN) varied from 0 nm to 4 nm in step size of 1 nm.

In Figure 4. It is shown Off-state current for both gate length. Underlap length (L_{UN}) varied from 0 nm to 4 nm. We get the lowest off-state current value, $I_{OFF} = 3.32\times10^{-9}$ A/um for L_{UN}= 4 nm and L_G=10 nm. From the figure it can be determined that as the L_{UN} increases the coupling capacitance getting reduced hence the I_{OFF} value decreases. For L_{UN}= 0 nm the highest off current was found.

Fig. 5. Shows I_{ON}/I_{OFF} ratio variation with L_{UN} of gate length 10 nm and 9 nm devices. The maximum attainable I_{ON}/I_{OFF} ratio value is 1.56×10^{6} for L_G =10 nm with L_{UN} = 4 nm is better than L_{UN} = 0 nm.

The sub-threshold slope can be evaluated as,

$$SS = \frac{\Delta V_g}{\Delta(\log I_d)} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (1)$$

Fig 6. Shows the variation in SS with underlap length of gate length 9 nm and 10 nm. The insertion of a barrier layer causes the channel to move away from the gate dielectric interface, reducing the electrostatic control and thus degrading the SS. An SS is observed to decrease linearly with an increase in L_{UN}. The observed SS values are nearly same as the ideal 60 mV/decade value.

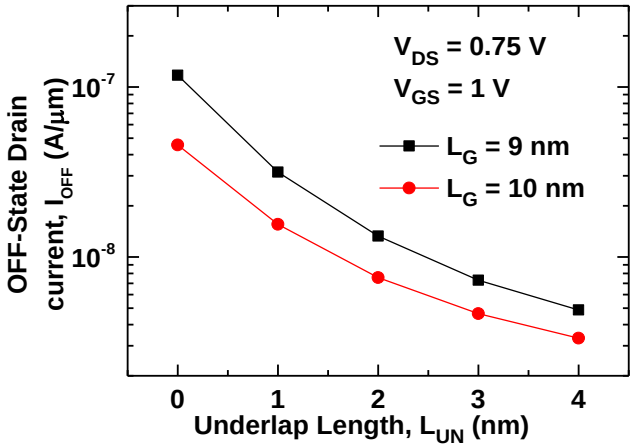

Fig. 4. IOFF vs. underlap length of gate length 10 nm and 9 nm. The underlap length (LUN) varied from 0 nm to 4 nm in step size of 1 nm.

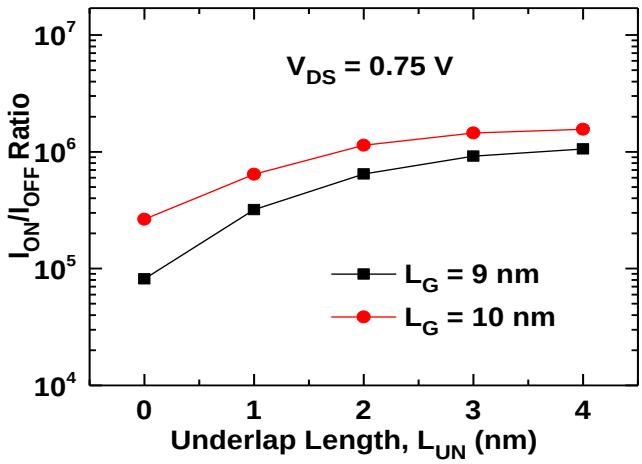

Fig 5. The ratio of ION/IOFF as a function of the underlap length (LUN).

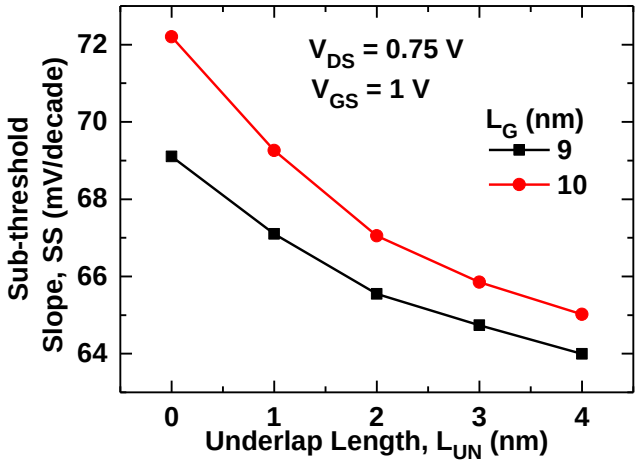

Fig. 6. Dependence of sub-threshold slope on underlap length.

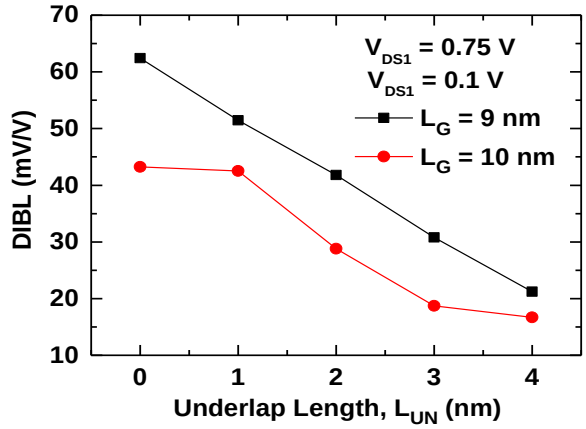

Fig 7. Variation of DIBL with LUN, where LUN is varied from 0 nm to 4 nm.

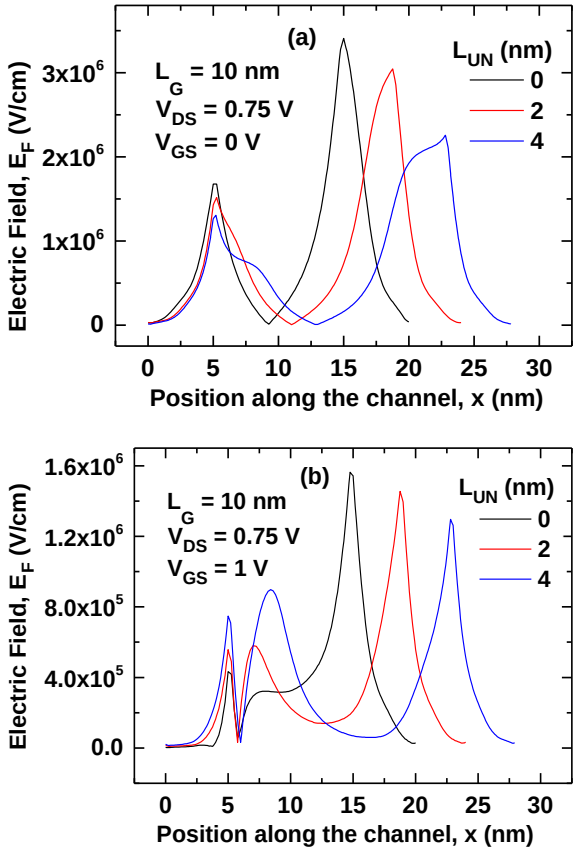

Fig 8. The electric field while drain voltage 0.75 V of 10 nm gate length device (a) at OFF-state (b) at ON-state.

The important parameter describing electrostatic integrity of MOSFETs is drain induced barrier lowering (DIBL), which is expressed as the shift of threshold voltage due to change in the drain voltage. The DIBL can be calculated as

$$DIBL = \frac{\Delta V_{th}}{\Delta V_{ds1}} = \frac{V_{th1} - Vt_{h2}}{V_{ds1} - V_{ds2}} \cdots\cdots\cdots\cdots (2)$$

Where Vth1 is threshold voltages extracted at a drain bias of V_{DS1} = 0.1 V and V_{TH2} are the threshold voltages extracted at a drain bias of V_{DS2} = 0.75 V. Fig. 7. Shows DIBL for varying L_{UN} of L_G = 10 nm and L_G = 9 nm. As L_{UN} increases from 0 nm (without underlap) to 4 nm, the drain and source region moves away from the gate and the effect of drain potential on channel decrease. As the drain region moves apart, barrier lowering caused by the drain decreases and thus DIBL decreases. DIBL for L_G=10 nm device decreases from 43.2 mV/V (L_{UN} = 0 nm) to 16.7 mV/V (L_{UN} = 4 nm).

Fig. 8 (a) and (b) represents the electric fields versus position along the direction of the channel of 10 nm device at OFF-state and ON-state respectively. In short channel MOSFETs of sub-10 nm regime there is fringing electric fields from source/drain region that penetrates through the channel and dielectric and affects the channel potential thereby the gate control is reduced [23]. Though there is High-K dielectric material for good gate control, underlap increases the effective channel length that shrinks the fringing electric field or short channel effects.

4. CONCLUSION

A performance investigation of GaN-based underlap DG-MOSFETs is done for major device metrics like DIBL, SS, I_{ON}/I_{OFF} and V_{TH} for a range of underlap and gate lengths. An impressive drain current density of 12 mA/μm is obtained for the device with a gate length of 10 nm and underlap length 0 nm. DIBL dependence on L_{UN} and becomes less for a longer underlap. The SS performance is degraded because the buried channel is away from the gate dielectric interface. Furthermore, underlap is found to be very effective in increasing V_{TH} for shorter underlap (up to 3 nm). Despite the higher I_{ON}, the I_{ON}/I_{OFF} ratio is getting higher due to decreasing I_{OFF}. The GaN-based underlap DG-MOSFETs shows excellent promise as one of the candidates to substitute present MOSFETs for future high-speed applications.

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