Analysis of 6T SRAM Cell in Different Technologies

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ABSTRACT
Static random access memory (SRAM) is an important component of embedded cache memory of handheld digital devices. SRAM has become major data storage device due to its large storage density and less time to access. Exponential growth of low power digital devices has raised the demand of low voltage low power SRAM. This paper presents design and implementation of 6T SRAM cell in 180 nm, 90 nm and 45 nm standard CMOS process technology. The simulation has been done in Cadence Virtuoso environment. The performance analysis of SRAM cell has been evaluated in terms of delay, power and static noise margin (SNM).

Keywords
Static RAM, Static Noise Margin, LLC -HVT

1. INTRODUCTION
In many digital systems, semiconductor memory arrays are capable of storing a large amount of data. The number of transistors used for the storage purpose is larger than the transistors used in logic operation and other purpose. The increasing demand of large storage capacity has driven the fabrication technology and compact size. The data storage capacity of semiconductor memory array approximately doubles in every two years. The area efficiency of the memory array is the number of storage bits per unit area is a key design factor which determines the total storage capacity. The important factor is required time to store and retrieve data in a memory array. SRAM is used in hard disk buffer, router buffer and CPU register and in some printers and LCD screen to display on print the image. In some cases SRAM is used as main memory like in previous computer i.e ZX80. SRAM is used in aerospace, medical science because here the data storage is critical and battery is impractical. SRAM is mostly used in cache memory in microprocessors, memory in devices due to high speed and high power consumption. SRAM is a type of semiconductor memory which store each bit. By using BJT SRAM can be designed but it has higher switching losses. Nowadays, SRAM is designed by using MOSFET which is low switching losses. Due to the technology scaling of CMOS devices in the nanometer era static or leakage power consumption dominates dynamic power dissipation. Dynamic power loss is due to the switching characteristics of transistor. So, designer should manage both static and dynamic power to improve the battery life. This work will provide guidelines to the researchers related to SRAM design.

2. BACKGROUND WORK
As the speed of the processor and main memory increases but power dissipation is an important factor. Now most of the research is for low power device.

2.1 Power Dissipation
Power dissipation in CMOS circuits is categorized in two types i.e. dynamic power and static power. It is the rate of energy which is consumed from the source and converted into heat. Dynamic power is due to the switching behavior of the transistor which is charging and discharging of load capacitance. Static power dissipation is due to the leakage current produces continuously from the power supply.

Power dissipation can be minimized by different techniques. Low power supply voltage (VDD) is one of the most widely used technique to achieve low power dissipation. When low supply voltage is applied to SRAM it improves battery life. The power dissipation produces less heat. But it has been observed that decreasing supply voltage [11] the RAM cell stability and delay are affected seriously. Many factors which are responsible for leakage current such as sub threshold leakage, drain induced barrier lowering, gate induced drain current, gate oxide tunneling, hot carrier effect [11].

3. MOTIVATION TOWARDS WORK
Intel microprocessors family demonstrates that on-chip memory cache size increases with increasing speed. On-chip level two cache size in Intel’s Pentium III Coppermine is increased from 256 KB to 4 MB in Intel’s core i3 processor, to 8 MB in Intel core i7-920 processor with 2.66 GHZ clock frequency. Also, in smart phone processor size of Qualcomm’s snapdragon processor family shows level two cache size increasing from 256 KB in Qualcomm QSD8250 WITH 65-nm technology, to 1 MB in Qualcomm S4- MSM8960 with 1.3 GHZ clock frequency.

For high performance microprocessor and system-on-chip (SoC) implementations larger sized on-chip caches are required. These large sizes consist of small SRAM memory blocks which are nothing but the array of SRAM memory cells. SRAM cells are arranged in such a way that bit line delay and word line delay due to the interconnection and parasitic capacitance will be low.

With technology scaling transistor sizes reduced by a factor of 2 in every 18 months. In comparison with transistor, interconnection are getting worse. Distributed interconnection delay dominates SRAM character. SRAM performance depends on the exact calculation of interconnection delay.

4. DIFFERENT CIRCUIT APPROACHES
Ajoy C A et al. [1]. The conventional SRAM design consists of six transistors which consumes more power and stability for read operation is less [1]. Here, the low power techniques are used which reduce the power consumption. Here, the low power logic is used as sleepy approach. In this approach an additional “sleep” PMOS transistor is placed between VDD and pull up network and an additional “sleep” NMOS
transistor is placed between the pull down network and ground (GND). The current mirror sensing amplifier is used for read operation. Using Cadence software schematic is drawn and power consumption is analyzed. The novel SRAM provides minimum power consumption.

Debiprasad Priyabrat Acharya et al. [2]. Here, two novel 8T SRAM cells, low leakage current SRAM cell and low leakage current high threshold voltage SRAM cell are proposed to offer high energy efficiency. The cell performance is compared with 8T SRAM and 6T SRAM cell. The proposed SRAM cell reduce the overall power consumption. During the high frequency access of SRAM the number of transition are high. The dynamic power consumption dominates the static power consumption. In this paper the researches proposed a cell which reduces both the static and dynamic power. The proposed cell is low leakage current SRAM (LLC-SRAM) cell. Here, overall power dissipation can be reduced due to reduction of dynamic power.

The work presented the following advantages:-

- The SRAM cell proposed here which can operate in wide frequency range of access. In both high frequency and low frequency the overall power can be consumed.
- It offers a quite good read stability as compare to conventional 6T SRAM cell.
- In the proposed SRAM cell the write operation is faster than 6T SRAM cell and read operation are nearly in same delay.

Xu Wang et al. [3]. Bit line toggling of SRAM system in write operation gives the largest portion of power dissipation. To reduce this amount of power loss here a new SRAM design is proposed that integrates charge pump circuits to reuse the bit line charge. After the simulation 11% power saving and 3.8% of area overhead are achieved.

Vijay Singh Baghel et al. [4], SRAM is memory which have a link with CPU. Designing of SRAM is difficult because it consumes large amount of power and area. So, to achieve low power a memristor based SRAM is proposed here. Memristor is a forth missing non-linear resistor which acts as memory and it improves the power and speed. MTCMOS (Multi Threshold CMOS) technique is used in this paper. It is a power reducing technique that helps in reducing leakage power in the SRAM by turning of the inactive circuit domains. Memristor based MTCMOS implemented in Cadence Virtuoso tool with 45 nm technology with supply voltage of 0.7 volt.

Abhishek Agal et al.[5]. The main objective of this paper is evaluating performance in terms of power consumption, delay and SNM of existing 6T CMOS SRAM cell in 45nm and 180 nm technology.

Sagar Josi et al.[6]. Here, in this paper the conventional 6T SRAM cell is modified with sense amplifier which improves the differential voltage of bit lines. Due to common mode rejection differential bit lines is used. Because of this we can reduce the effect of noise and signal degradation. The modified 6T SRAM cell is analyzed by varying different temperature and power supply by using Cadence tool.

Pankaj Agrawal et al. [7]. Leakage current is an important part of power loss. Here, some techniques are proposed that reduces the leakage current. Leakage current is a major part in standby mode. Different parameter of CMOS transistor is responsible for power consumption. The leakage current in process can be decreased use deep sub micron method. Here 7T SRAM cell using a techniques where both circuit level, process level in one cell as hybrid cell.

Gonzalo ELisa Blanco silva et al.[8]. This paper represents a digital device using FPGA technology for image processing. The image is sent from PC to digital system using RS232 interface. Image is stored in flash memory and it is translated to SRAM memory then processes it and display by VGA interface. The proposed architecture is described in hardware description language by standard VHDL. The architecture is tested by an image and the result is compared with the Matlab result.

Jianxing Wang et al. [9], STT-RAM is a NVRAM. Which having high density, low power and having a very good speed as compared to conventional SRAM cell. In this paper a hybrid L1 cache architecture is proposed which is an integral of both SST-RAM and NVRAM. As compared to the conventional SRAM design, the proposed SRAM consumes 38% of energy.

K. Dhanumjaya et al. [10], proposed a design of low power SRAM which contains decoder, sense amplifier and TG gates in cadence tool at 45nm technology.

5. 6T SRAM CELL
The 6T SRAM cell consist of 6 MOSFET where 4 transistors are coupled as CMOS inverter, here bit is stored as 1 or 0 and other two transistor is act as pass transistor to control the SRAM cell by bits line. When WL(word line) is high then the SRAM cell can be accessed.

![Fig.1 6T SRAM cell](image)

5.1 Standby mode
In standby mode word line WL is 0 then the two pass transistor N3 and N4 is off and the SRAM cell cannot be accessed and the contents of coupled transistor is remain unchanged as long as supply voltage exist.

5.2 Read mode
In read mode WL is selected and it enables the two pass transistors which are connected to the bit lines. Now the value stored at node A and B are transferred to the bit lines.1st assume 1 is stored at node so the BL will discharge through the N1 and the BL is pull up through P1 to VDD. In this mode of operation P1 and N2 transistors are turned off but the transistors N1 and P2 are operate in linear mode. The inactive transistors at the beginning of the data read operation are shown in Fig.2 with cross mark.
5.3 Write mode
In this mode $\overline{BL}$ and BL is charged to Vdd. To written something in SRAM either $\overline{BL}$ and BL is discharge to ground. If 1 is need to write BL is charged to Vdd and $\overline{BL}$ is discharged through ground. If logic 0 has to written $\overline{BL}$ charged to Vdd and BL is discharge through ground, then the WL gets active and data is written in to the cell. The inactive transistors at the beginning of the data write operation are shown in fig.3 with cross mark.

6. RESULT ANALYSIS
6.1 Design of 6T SRAM Cell in 180 nm, 90nm and 45nm technology
6T SRAM cell has been designed in 180 nm, 90 nm and 45 nm technology using Cadence Virtuoso tool which are shown in Fig.4, Fig.5 and Fig.6.

6.2 Delay analysis
Calculating the delay for each 6T SRAM cell in 180nm,90nm,45nm technology. Delay time depends on the critical voltage and W/L ratio of the transistors.

In this work, in 180nm technology the supply voltage is 1.8V, in 90nm technology the supply voltage is 1.2V and in 45nm technology the supply voltage is 0.5 V.
6.3 Delay analysis

Delay for each 6T SRAM cell in 180nm, 90nm and 45nm technology has been calculated and shown in Table 1. Delay time depends on the critical voltage and W/L ratio of the transistors.

<table>
<thead>
<tr>
<th>Technology</th>
<th>Tfall</th>
<th>Trise</th>
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</thead>
<tbody>
<tr>
<td>180 nm</td>
<td>103.7p</td>
<td>327.1p</td>
</tr>
<tr>
<td>90 nm</td>
<td>87.8p</td>
<td>732.1p</td>
</tr>
<tr>
<td>45 nm</td>
<td>326.6p</td>
<td>354.9p</td>
</tr>
</tbody>
</table>

6.4 Power analysis

Power has been calculated with the help of Cadence tool. The calculated power is given in Table 2. Table 2 shows that the power dissipation reduces with the scaling of technology. The power dissipation depends on the supply voltage and parameter.

<table>
<thead>
<tr>
<th>Technology</th>
<th>Power (WATT)</th>
</tr>
</thead>
<tbody>
<tr>
<td>180 nm</td>
<td>519.7 n</td>
</tr>
<tr>
<td>90 nm</td>
<td>59.580 n</td>
</tr>
<tr>
<td>45 nm</td>
<td>30.68 n</td>
</tr>
</tbody>
</table>

6.5 Static Noise Margin (SNM)

SNM is static noise margin. The maximum DC voltage can be condensed by the SRAM cell without affecting the stored bit. The SNM can be achieved by DC analysis. The SNM is calculated and given in Table 3.

<table>
<thead>
<tr>
<th>Technology</th>
<th>SNM for read operation</th>
<th>SNM for write operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>180nm</td>
<td>0.35 v</td>
<td>0.31 v</td>
</tr>
<tr>
<td>90nm</td>
<td>0.17 v</td>
<td>0.07 v</td>
</tr>
<tr>
<td>45nm</td>
<td>0.14 v</td>
<td>0.19 v</td>
</tr>
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7. CONCLUSION

In this paper the simulation is done by using Cadence Virtuoso tool. The simulation is done for 6T SRAM cell in 180nm, 90nm and 45nm technology node. The design architecture shows speed improvements along with scaling of technology and delay time also decrease. Power dissipation also decreases with scaling of technology. Simulation and result analysis are done in terms of power dissipation, delay and SNM.

8. ACKNOWLEDGMENTS

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9. REFERENCES


